Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **N. MR**
2. **CP**
3. **P0**
4. **P1**
5. **P2**
6. **P3**
7. **PE**
8. **GND**
9. **N. SPE**
10. **TE**
11. **Q3**
12. **Q2**
13. **Q1**
14. **Q0**
15. **TC**
16. **VCC**

**.064”**

**13**

**12**

**11**

**7 8 9 10**

**2 1 16 15 14**

**3**

**4**

**5**

**6**

**13636D**

**MASK**

**REF**

**.074”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size = .004 x .004”**

**Backside Potential: ISOLATED**

**Mask Ref: 13636D**

**APPROVED BY: DK DIE SIZE .064” X .074” DATE: 5/20/19**

**MFG: T.I./HARRIS THICKNESS .021” P/N: 54HCT163**

**DG 10.1.2**

#### Rev B, 7/1